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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/729,010	12/04/2000	Michael Ficco	PD-200235	6750

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EXAMINER	
HOFFMAN, BRANDON S	

ART UNIT	PAPER NUMBER
2136	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/729,010	FICCO, MICHAEL	
	Examiner	Art Unit	
	Brandon Hoffman	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-9,12,17-20,33,37-42,44,48-51 and 54-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-9,12,17-20,33,37-42,44,48-51 and 54-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1, 5-9, 12, 17-20, 33, 37-42, 44, 48-51, and 54-69 are pending in this office action.

2. Applicant's arguments filed June 30, 2004, for a request for reconsideration has been granted. A new ground of rejection has been made.

Rejections

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

4. Claims 1, 5-9, 12, 17-20, 33, 37-42, 44, 48-51, 54-57, 59-63, and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto et al (U.S. Patent No. 5,796,828) in view of Yim (U.S. Patent No. 6,810,387).

Regarding claims 1, 33, and 44, Tsukamoto et al. teaches a method/apparatus for storing and retrieving digital data within a hardware platform (figure 2), the method comprising:

- Receiving data bits across a bus, the data bits forming a bit pattern (figure 2, reference numbers 103 and 20);
- Altering the bit pattern of the data bits (figure 2, reference number 22);

- Storing the altered data bits (figure 2, reference numbers 23A, 24, and 40);
- Restoring the altered data bits to the bit pattern (figure 2, reference number 25); and
- Outputting the restored data bits (figure 2, reference numbers 26 and 105).

Tsukamoto et al. does not teach wherein the altering comprises one of inverting bits in selected bit positions of the data bits and scrambling bits in the selected bit positions of the data bits to prevent unauthorized use of the data bits.

Yim teaches wherein the altering comprises one of inverting bits in selected bit positions of the data bits and scrambling bits in the selected bit positions of the data bits to prevent unauthorized use of the data bits (col. 3, line 65 through col. 4, line 38).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine wherein the altering comprises one of inverting bits in selected bit positions of the data bits and scrambling bits in the selected bit positions of the data bits to prevent unauthorized use of the data bits, as taught by Yim, with the method/apparatus of Tsukamoto et al. It would have been obvious for such modifications because inverting/scrambling bits in selected bit positions prevents the data from being copied off of a hard disk drive (see col. 3, line 65 through col. 4, line 38 of Yim).

Regarding claim 5 and 37, the combination of Tsukamoto et al. in view of Yim teaches wherein the altering and the restoring are performed by a hard disk drive interface (see figure 2, reference number 23A of Tsukamoto et al.).

Regarding claims 6, 7, 17, 18, 38, 39, 48, 49, 55, and 60, the combination of Tsukamoto et al. in view of Yim teaches wherein the altering is unique to the hardware platform/plurality of platforms (see col. 4, lines 2-5 of Yim, by using the serial number of a device for altering, wherein the serial number is unique (or at least relatively unique), the altering will be unique to each device, and therefore unique to the hardware platform.).

Regarding claims 8, 19, 40, 50, 56, and 61, the combination of Tsukamoto et al. in view of Yim teaches wherein the altering is based upon a serial number of the hardware platform (see col. 4, lines 2-5 of Yim).

Regarding claims 9, 20, 41 51, 57, and 62, the combination of Tsukamoto et al. in view of Yim teaches (a processor coupled to the system bus for) generating a random number upon power-up of the hardware platform, wherein the altering is based upon the random number (col. 4, lines 16-19).

Regarding claim 12, Tsukamoto et al. teaches an apparatus for storing and retrieving digital video data (figure 2), comprising:

- A system bus configured to transfer data bits, the data bits forming a bit pattern (figure 2, reference numbers 103, 20 and 21A);
- An interface coupled to the system bus and configured to alter the bit pattern of the data bits (figure 2, reference numbers 22, 23A, and 25); and
- A hard disk drive coupled to the interface and configured to store the altered data bits (figure 2, reference number 40).

Tsukamoto et al. does not teach wherein the interface is configured to alter the bit pattern by one of inverting bits in selected bit positions of the data bits and scrambling bits in the selected bit positions of the data bits to prevent unauthorized use of the data bits.

Yim teaches wherein the interface is configured to alter the bit pattern by one of inverting bits in selected bit positions of the data bits and scrambling bits in the selected bit positions of the data bits to prevent unauthorized use of the data bits (col. 3, line 65 through col. 4, line 38).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine wherein the interface is configured to alter the bit pattern by one of inverting bits in selected bit positions of the data bits and scrambling bits in the selected bit positions of the data bits to prevent unauthorized use of the data bits, as taught by Yim, with the method/apparatus of Tsukamoto et al. It would have

been obvious for such modifications because inverting/scrambling bits in selected bit positions prevents the data from being copied off of a hard disk drive (see col. 3, line 65 through col. 4, line 38 of Yim).

Regarding claim 42, the combination of Tsukamoto et al. in view of Yim teaches wherein the altered data bits are stored on a hard disk drive (see column 4, lines 19-28 of Tsukamoto et al.).

Regarding claims 54 and 57, Tsukamoto et al. teaches a method for storing and retrieving digital data within a hardware platform (figure 2), the method comprising:

- Receiving a plurality of data bits, the data bits forming a bit pattern (figure 2, reference numbers 103 and 20);
- Altering the bit pattern (figure 2, reference number 22);
- Storing the altered bit pattern on a medium (col. 4, lines 19-21);
- Retrieving the stored altered bit pattern from the medium (col. 4, lines 21-24);
- Restoring the altered bit pattern by inverting the bits (figure 2, reference num 25); and
- Outputting the restored data bits (figure 2, reference numbers 26 and 105).

Tsukamoto et al. does not teach altering by inverting bits in a first selection of bit positions of the data bits/scrambling bits of selected bit positions of the data bits, and

restoring the bits of the first selection of bit positions of the retrieved bit pattern/unscrambling the bits of the selected bit positions of the retrieved bit pattern.

Yim teaches altering by inverting bits in a first selection of bit positions of the data bits/scrambling bits of selected bit positions of the data bits, and restoring the bits of the first selection of bit positions of the retrieved bit pattern/unscrambling the bits of the selected bit positions of the retrieved bit pattern (col. 3, line 65 through col. 4, line 38).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine altering by inverting bits in a first selection of bit positions of the data bits/scrambling bits of selected bit positions of the data bits, and restoring the bits of the first selection of bit positions of the retrieved bit pattern/unscrambling the bits of the selected bit positions of the retrieved bit pattern, as taught by Yim, with the method/apparatus of Tsukamoto et al. It would have been obvious for such modifications because inverting/scrambling bits in selected bit positions prevents the data from being copied off of a hard disk drive (see col. 3, line 65 through col. 4, line 38 of Yim).

Regarding claim 63, Tsukamoto et al. teaches a method for storing and retrieving digital data within a media receiver, the method comprising:

- Receiving a plurality of data bits from a service provider, the data bits forming a bit pattern (fig. 2, ref. num 103 and 20);

- Altering the bit pattern without receiving from the service provider a control signal indicative of a characteristic associated with storing the bit pattern on a medium (fig. 2, ref. num 22);
- Storing the altered bit pattern on the medium (fig. 2, ref. num 23A, 24, and 40);
- Retrieving the stored altered bit pattern from the medium (fig. 2, ref. num 25);
- Restoring the altered bit pattern (fig. 2, ref. num 25); and
- Outputting the restored bit pattern (fig. 2, ref. num 26 and 105).

Tsukamoto et al. does not teach wherein the altering comprises without receiving from the service provider a control signal indicative of a characteristic associated with storing the bit pattern on a medium.

Yim teaches wherein the altering comprises without receiving from the service provider a control signal indicative of a characteristic associated with storing the bit pattern on a medium (col. 3, line 65 through col. 4, line 38).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine wherein the altering comprises wherein the altering comprises without receiving from the service provider a control signal indicative of a characteristic associated with storing the bit pattern on a medium, as taught by Yim, with the method/apparatus of Tsukamoto et al. It would have been obvious for such modifications because the signal could be seen and compromised.

Regarding claim 69, the combination of Tsukamoto et al. in view of Yim teaches wherein the media receiver comprises at least one of a tuning device, a digital video recording device, and a personal computer (see col. 3, lines 10-12 of Yim).

Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto et al (USPN '828) in view of Yim (USPN '387), and further in view of Gannett (U.S. Patent No. 3,944,745).

Regarding claim 58, the combination of Tsukamoto et al. in view of Yim teaches all the limitations of claim 54, above. However, the combination of Tsukamoto et al. in view of Yim does not teach wherein the altering further comprises scrambling bits of a second selection of bit positions of the bit pattern, and the restoring further comprises unscrambling the bits of the second selection of bit positions of the retrieved altered bit pattern.

Gannett teaches wherein the altering further comprises scrambling bits of a second selection of bit positions of the bit pattern (fig. 7A), and the restoring further comprises unscrambling the bits of the second selection of bit positions of the retrieved altered bit pattern (fig. 7B).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine scrambling bits of a second selection of bit positions

and unscrambling bits of the second selection, as taught by Gannett, with the method/apparatus of Tsukamoto et al./Yim. It would have been obvious for such modifications because a second round of scrambling will provide even more security. Although the reference shows an analog scrambling method, it would have been obvious to apply the method of Gannett to a digital data. Also, the concept of altering/scrambling selected bits is taught in claim 54, above. Gannett merely provides the missing feature, more precisely, Gannett teaches altering/scrambling a second selection of data and restoring a second selection of data.

Claims 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto et al (USPN '828) in view of Yim (USPN '387), and further in view of LaBerge (U.S. Patent No. 6,795,931).

Regarding claim 64, the combination of Tsukamoto et al. in view of Yim teaches all the limitations of claim 63, above. However, Tsukamoto et al./Yim does not teach wherein altering the bit pattern comprises inverting at least one bit in a selected bit position of the data bits via at least one inverter.

LaBerge teaches wherein altering the bit pattern comprises inverting at least one bit in a selected bit position of the data bits via at least one inverter (fig. 4).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine inverting the selected bits by an inverter, as taught by LaBerge, with the method/apparatus of Tsukamoto et al./Yim. It would have been obvious for such modifications because inverting bits provides a different result, which would alter the original data; this provides security of data.

Regarding claim 65, the combination of Tsukamoto et al. in view of Yim teaches all the limitations of claim 63, above. However, Tsukamoto et al./Yim does not teach wherein altering the bit pattern comprises: receiving the plurality of data bits from a bus, each of the plurality of data bits corresponding to one of a plurality of lines associated with the bus; selecting at least one of the plurality of lines to form a line selection; and inverting at least one of the plurality of data bits based on the line selection.

LaBerge teaches wherein altering the bit pattern comprises: receiving the plurality of data bits from a bus, each of the plurality of data bits corresponding to one of a plurality of lines associated with the bus (fig. 4, ref. num 312); selecting at least one of the plurality of lines to form a line selection (fig. 4, ref. num 310); and inverting at least one of the plurality of data bits based on the line selection (fig. 4, ref. num 400, 402).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine receiving data bits over a plurality of lines, selecting at least one line, and inverting the bits based on the line selection, as taught by LaBerge,

with the method/apparatus of Tsukamoto et al./Yim. It would have been obvious for such modifications because inverting bits provides a different result, which would alter the original data; this provides security of data.

Regarding claim 66, the combination of Tsukamoto et al./Yim in view of LaBerge teaches wherein selecting the at least one of the plurality of lines to form the line selection comprises selecting the at least one of the plurality of lines based on at least one of a random number and a serial number associated with the media receiver (see col. 3, line 65 through col. 4, line 38 of Yim).

Regarding claim 67, the combination of Tsukamoto et al./Yim in view of LaBerge teaches wherein selecting the at least one of the plurality of lines to form the lines selection comprises controlling at least one of a plurality of multiplexers to form the line selection, and wherein each of the plurality of multiplexers corresponds to one of the plurality of lines (see fig. 4, ref. num 302, 304, 306 of LaBerge).

Regarding claim 68, the combination of Tsukamoto et al./Yim in view of LaBerge teaches wherein each of the plurality of lines is associated with an inverter (see fig. 4, ref. num 400, 402 of LaBerge).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon Hoffman whose telephone number is 571-272-3863. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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